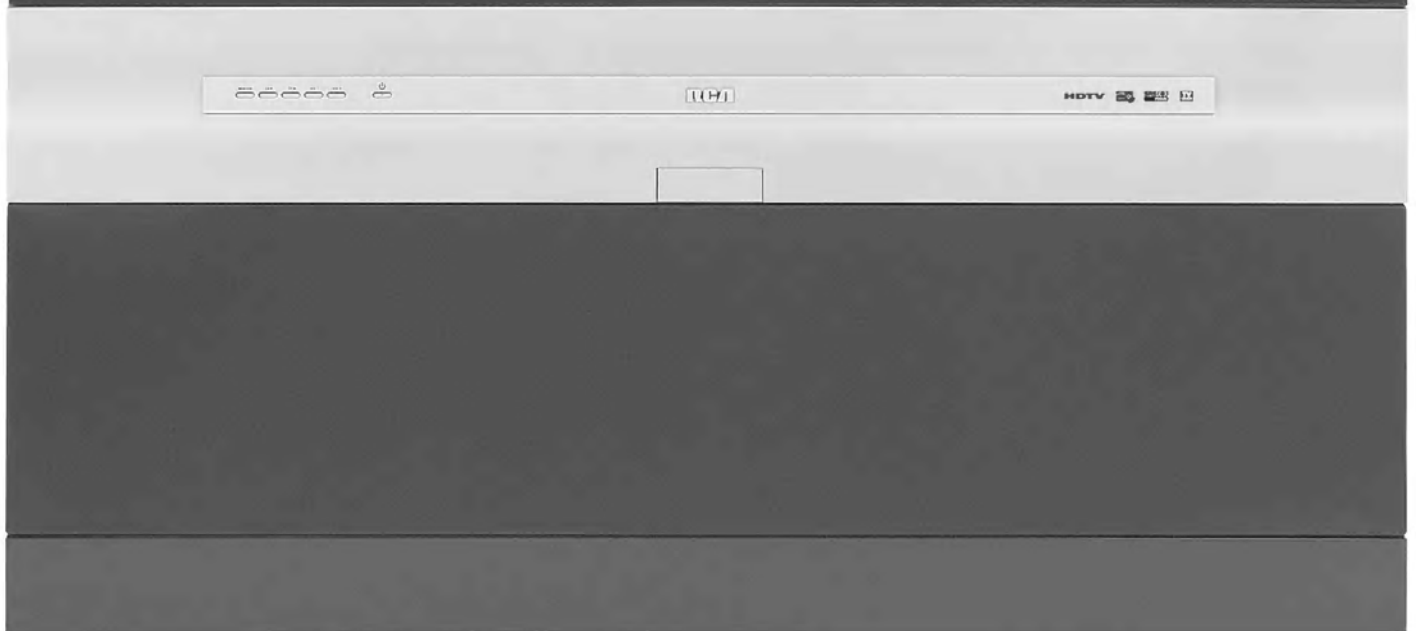


RCA SCENIUM

ATC321 PTV
Training Manual
Supplement
to
ATC32x DLP Training Manual



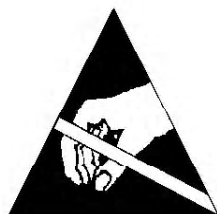
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FOREWORD

The ATC321 training manual is an supplement to the ATC32x DLP Training Manual designed to provide the service technician with information key to the servicing of the PTV chassis. This training manual is to be used in conjunction with the ATC32x Training manual, and additional information found in the ESI Service Data.

SAFETY INFORMATION CAUTION

Safety information is contained in the appropriate Thomson Service Data. All product safety requirements must be complied with prior to returning the instrument to the consumer. Servicers who defeat safety features or fail to perform safety checks may be liable for any resulting damages and may expose themselves and others to possible injury.



All integrated circuits, all surface mounted devices, and many other semiconductors are electrostatically sensitive and therefore require special handling techniques.

RCA

RCA SCENIUM

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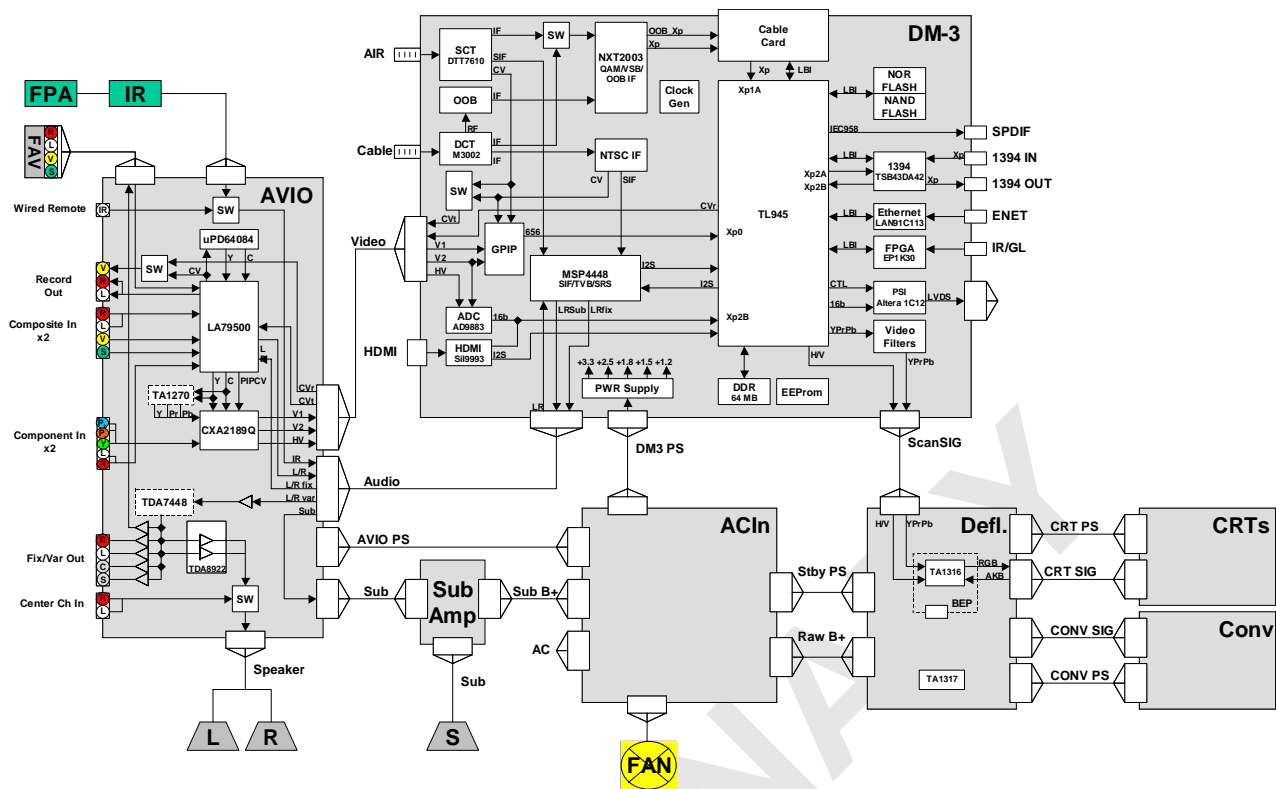
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Overview

The ATC321 chassis is modular with separate circuit board assemblies (CBA) for various circuits.

The major CBA's are:

- AC IN
- Deflection
- Audio
- A/V In
- Convergence
- DM3
- Back End Processor (BEP)
- CRT CBA's (Red, Green, and Blue)

The cabinet is also a modular design with the "Box" (screen, frame, and mirror) able to be separated from the lower cabinet assembly that houses the PTV kit. This allows easy access to the chassis for servicing. See service positions for more information.

AC In CBA

The AC in CBA provides the standby power supplies +33V, -5V, +12V, +5V, and audio +/- 21V. Raw B+ is also provided to the main chassis.

Deflection CBA

The deflection CBA or main chassis contains the run supply, back end processor (BEP), horizontal and vertical circuits. The BEP and deflection CBA are aligned together and therefore are married and can only be replaced together. The BEP is a module like the DM2 but the deflection CBA is component level serviceable.

Audio CBA

The audio CBA contains audio processing, final amp and speaker output. The left and right audio signals from the AV CBA are processed and routed to the internal or external speakers by the Audio CBA. Power for the Audio CBA is + / - 21Vdc from the standby power supply CBA.

A/V In CBA

Audio and Video switching is done on the A/V In CBA. Further video processing (comb filtering and PIP) is also done on the A/V In CBA. The DVI input, switching, and processing is part of the A/V In CBA. Outputs are 2-2.14H YPrPb, 1H YPrPb, Composite video, and audio. All NTSC signals are processed and switched to the DM2 for up-conversion. The 2-2.14H YPrPb signals are switched and sent to the BEP for processing.

Convergence CBA

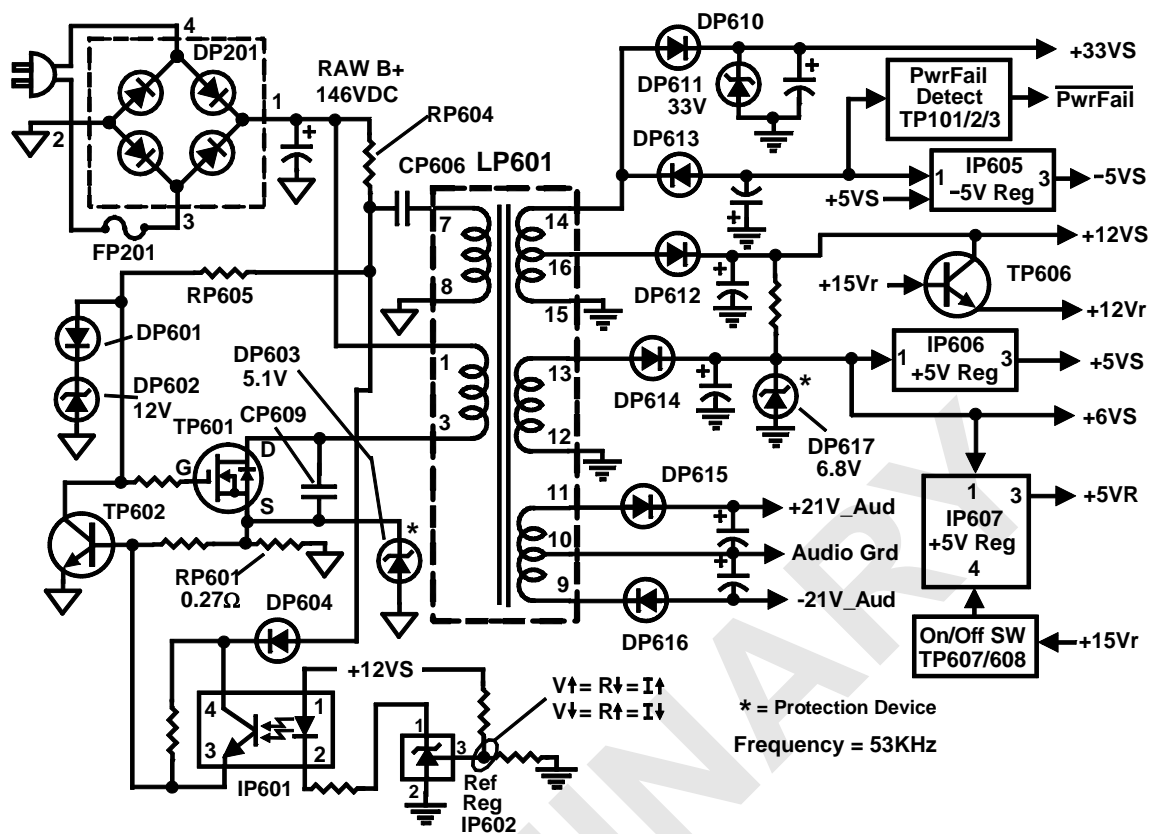
The convergence CBA houses convergence processing and the convergence amplifiers. Horizontal and vertical sync signals and power come from the deflection CBA. Alignment pattern and data are on the convergence CBA for auto-convergence and service adjustments.

DM3 Module

What goes on in the DM3 is digital processing of NTSC signals and AC3 audio processing. Main and PIP tuners, DTV links, and Ethernet processing is also contained in the DM3. The NTSC signals are digitally converted and up converted to 2.14H. Further processing takes the digital up-converted NTSC signal and passes it through a D/A converter to an YPrPb output at 2.14H. The YPrPb 2.14H signal is sent to the BEP for further processing. System control processing, user input, and Ethernet communication is also done by the DM3. Clock and data from the DM3 communicates with the deflection, A/V in, Audio, and convergence CBA's. This makes the DM3 the heart and brains of the ATC321.

CRT CBA

As with all projections there are three CRT drive CBA's, one for each color. Each CBA has a single Integrated Circuit that is used for the kine drivers. A current reference for AKB is DC coupled from each IC driver back to the back end processor. Grid Kick and Scan Loss provide protection from shutdown/ startup burns.



Standby Power Supply

Standby Power Supply Overview

The standby power supply is a PWM regulated, constant frequency (53KHz) power supply. When the unit is plugged into 120AC, startup resistor RP604 and RP605 provides the initial gate bias voltage which turns on the power output device (TP601) the first time. A positive feedback voltage is developed by windings between pins 7 & 8 of LP601. This positive voltage is capacitively coupled back to the gate of TP601. This causes TP601 to saturate and the voltage drop across the current sensing resistor RP601 turns on TP602. With TP602 on, the gate of TP601 is grounded shutting off the output device. When TP601 is turned off, the energy stored in the primary windings (LP601 pins 1 & 3) is transferred to the secondary

windings of LP601. When current through TP601 stops flowing, TP602 is turned off. When all the energy has been completely drained from the primary the gate is again pulled high which turns on TP601 for the next cycle.

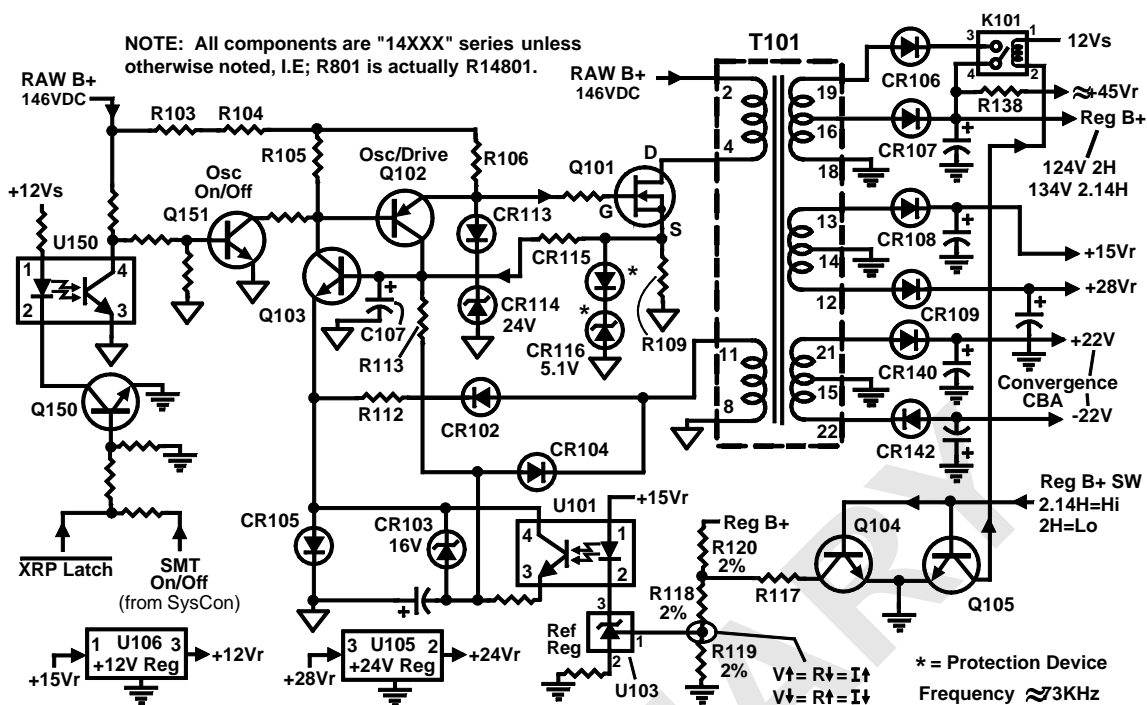
The standby supplies are generated by the rectifier diodes and filter capacitors on the secondary of LP601. This includes +33VS, -5VS, +12VS, +5VS, +6VS and the +/- 21 volt audio supply. The unregulated -5VS supply follows raw B+ and a power fail (active lo) signal is developed by transistors TP101, TP102 and TP103. Transistors TP101 & TP102 are normally on while TP103 is normally off. If Raw B+ (146VDC)

starts to fall, TP101 & 102 turn off which turns on TP103 generating the active low power fail signal that is applied back to the system control. Two switched run supplies are also generated by the standby supply. TP606 is turned on by the +15VR generating a +12VR supply.

A +5VR is provided by IP607. The +5VR run regulator is turned on by the On/Off switch transistors TP607 & 608. The transistors (TP607 & 608) are activated by the application of the +15VR run supply. Overvoltage protection in the secondary is provided by the 6.8V zener diode DP617. If the voltage rises above the 6.8V, the zener breaks over and clamps the output voltage.

Regulation of the supply is accomplished by Opto-Coupler IP601 and Ref Reg IP602. The bias supply for the photo transistor of IP601 is developed by diode DP604 from pulses off pin 7 of LP601. The +12VS is the supply that is monitored for regulation. The supply is regulated by varying the bias voltage on the base of TP602. A voltage divider network applies the reference voltage to pin 3 of the reference regulator IP602.

If the voltage at pin 3 of IP602 goes up (+12VS supply is increasing), the internal resistance of Ref Reg (IP602) goes down. This increases the current through the photodiode of IP601. When the current through the photo diode increases the current in the photo transistor increases and causes the base voltage of TP602 to go up. The increased base voltage on TP602 reduces the current sense (RP601) trip voltage which reduces the amount of 'On' time for TP601. This reduced 'On' time reduces the output power that is transferred to the secondary which in turn reduces the output voltages of the secondary. The opposite occurs if the supply output voltage is decreasing. The base bias voltage of TP602 is reduced allowing TP601 to stay on longer and pumping more power into the secondary which increase the output voltages. DP601 and DP602 (zener) provides the gate bias voltage of TP601. The 5.1V zener diode DP603 serves as a protective device in the event that TP601 is shorted and the current sense resistor opens, the zener breaks over and shorts to ground to allow the line fuse FP201 to open.



Main (Run) Power Supply

Main (Run) Power Supply Overview

The main (run) power supply is a constant frequency (approx. 73KHz) switch mode power supply that is regulated using pulse width modulation (PWM). The power supply is held off by Q151. Q151 is turned on during standby. With Q151 on, ground is applied to the base of Q102. With Q102 on, the gate of the power output (Q101) is held low preventing the supply from running.

The supply is turned on by the SMT On/Off signal from the system control and is applied to Q150. When Q150 turns on, ground is applied to pin 2 of U150. This causes the photo diode to conduct which in turn causes the photo transistor to saturate applying ground to pin 4 of U150. This turns off transistor Q151 and allows the oscillator driver (Q102/103) circuit to operate. In case of an XRP shutdown, the base of Q150 is

pulled low, shutting it off. With Q150 off, Q151 is allowed to turn back on which grounds the base collector junction of the oscillator driver Q102 & Q103 turning the run supply off.

Raw B+ (146VDC) is applied to the drain of Q101 via pin 2 & 4 of T101. After the oscillator drivers have been released by turning off Q151 the diodes CR114, CR113 and resistor R106 turns on the output device (Q101) for the first time. With Q101 turned on, energy is stored in the primary winding of T101 (pins 2 & 4). As the current through R109 (current sense resistor) increases a positive voltage is coupled to the base of Q103. Once this voltage is high enough, Q103 & Q102 removes the drive from the gate of Q101. Once Q101 is turned off, the energy stored in the primary windings (T101 pins 2 & 4) is transferred to the secondary windings

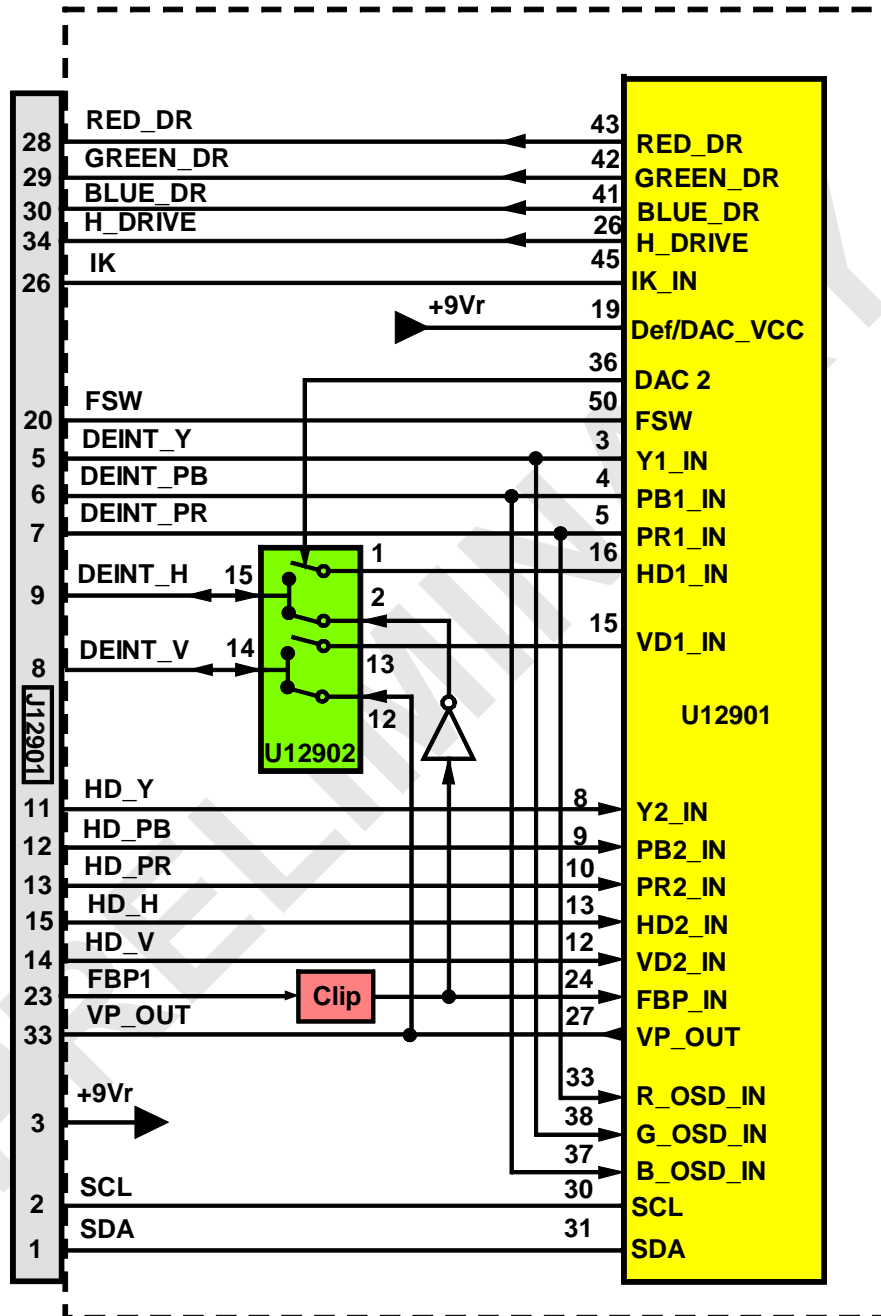
of T101. The diode CR105 provides the current path for Q103 during startup while CR114 and CR113 set the bias on the gate of Q101.

Diodes CR115 and CR116 serve as protection devices in the event that Q101 shorts and R109 opens. The diodes conduct applying ground to the source of Q101. This allows enough current to be drawn that the main fuse opens. Diode CR102 provides a positive re-supply voltage to the oscillator driver circuit. CR104 generates the negative supply for U101-3 and the base of Q103.

The rectifier diodes on the output of T101 generate the various run supplies needed by the chassis. Regulated B+ is generated by CR107. However, since the chassis operates at 2.14H (134V), a slightly different Reg B+ is needed. This is accomplished by the Reg B+ Switch signal from the system control that is applied to transistors Q104 and Q105. When Q104 is turned on the resistor divider network (R117/118/119 & R120) connected to pin 1 of the reference regulator (U103) is altered slightly to compensate for the slightly higher Reg B+. When Q105 is turned on the relay K101 is closed and switches in an additional source voltage rectifier (CR106) increasing Reg B+ slightly. With 2.14H operation requiring a slightly

higher Reg +. The Reg B+ Switch signal is Hi for 2.14H.

Reg B+ is monitored for regulation of the supply. U101, U103 and the precision resistor network serve as the regulation feedback circuit. As Reg B+ goes up or down, the voltage at pin 1 of U103 will go up or down as well. This changes the current flow through the photo transistor of U101. This causes the voltage on the emitter of Q103 to change. The voltage at the emitter of Q103 determines how long the output device stays on which determines the output power of the supply. For example, if the voltage at U103-1 rises, the resistance through the diode of U103 goes down allowing more current through the photo diode of U101. This causes the photo transistor to turn on harder causing the voltage at Q103-E to go more negative. This allows the oscillator driver to turn off Q101 sooner thus reducing the amount of power in the secondary. In reverse, if the voltage at U103-1 goes down the current through the photo diode goes down causing less current through the phototransistor. This allows the voltage at Q103-E to move in a positive direction. This causes the oscillator driver to keep Q101 on longer which increases the amount of power in the secondary. More power in the secondary causes the voltages to rise. Finally, U105 and U106 generate a +24Vr and +12Vr supplies from the +28Vr and +15Vr supplies respectively.



Back End Processor

Back End Processor (BEP)

Except for the de-interlacing, the luminance processing is done in U12901 back end processor BEP. U12901 has two component video inputs. YPrPb from the DM3 is on J12901 pins 5, 6, and 7. External 2H or 2.14H YPrPb is on J12901 pins 11, 12, and 13. The YPrPb signal undergoes the following processing within the BEP:

- Black Stretch
- Black Level Correction
- Dynamic Gamma Processing
- Controlled DC Restoration
- Sharpness Control
- Edge Replacement
- High Frequency White Peak Limiting
- Sub Contrast
- UniColor (Ganged Contrast and Color Level)
- Clamping
- White Peak Limiting
- Output Gamma Processing
- Half Tone Processing

OSD RGB Processing

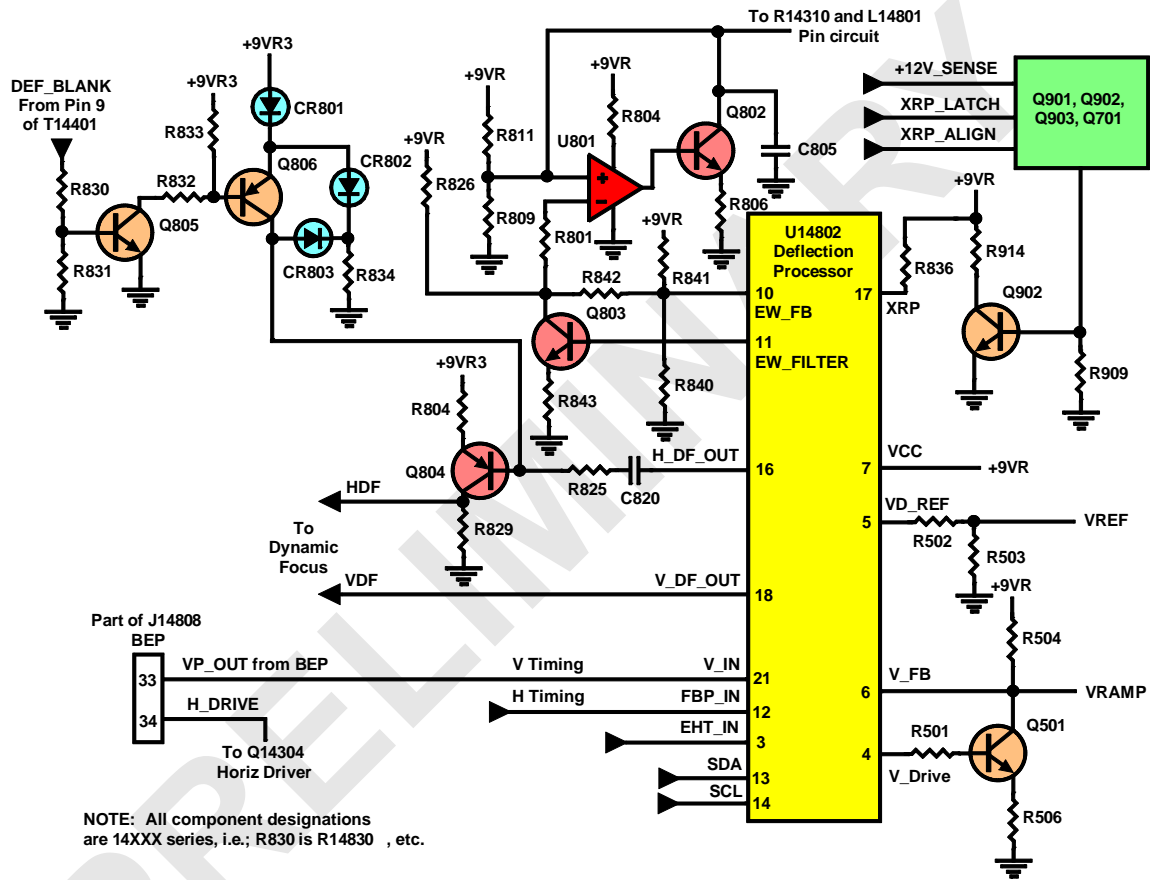
The OSD is processed and inserted by the DM2 for NTSC signals. Whenever an external 2H or 2.14H signal source (including DVI) is selected, the OSD is no longer part of the video. The OSD must be inserted to the external signal as an RGB signal from the DM3. The OSD RGB and fast switch signals are applied to U12901 from the DM3 via J12901 pins 5, 6, 7, 8 and 9. The fast

switch line (pin 20) controls the correct timing of OSD to video. There are two fast switch inputs on the Backend Processor; however, since there is only one fast switch line from the DM3, the two FSW inputs are tied together on the BEP board. When the OSD inputs to the Backend Processor are above 0.7 volts, the SVM output signal is disabled. After beam limiting, the OSD signal is mixed with the video RGB.

RGB Output Processing

The RGB signals from the OSD/Video RGB matrix are applied to variable gain stages, two of which are controlled by the bus. The ATC321 controls the gain of Red and Blue channels, leaving the Green channel at fixed gain. The gain of the amplifiers is adjusted to achieve the desired display color temperature. The gain of the Red and Blue are modified to change color temperature from Normal to Warm or Cool. To set the color temperature for Warm, the Red gain is increased and the Blue gain is reduced. To set the color temperature for Cool, the Red gain will be reduced and the Blue gain will be increased.

After the RGB signals are gain controlled, they are applied to a set of clamps. These clamps are used to set the output DC levels of the RGB signals. The video signals have horizontal and vertical blanking applied to them at the output buffers and is output on the RGB pins of the IC.



Deflection

Deflection

The ATC321 deflection consists of two levels, Low Level Deflection and the Output. Low level processing is done in part by the backend processor (U12901) and by U14802 deflection processor. The deflection processor U14802 generates the East West parabola, vertical ramp, and dynamic focus signals. The backend processor U12901 generates horizontal PLL, H/V countdown, and H / V drive signals. **H_DRIVE** from the Back End Processor is used to drive Q14304 and the Horizontal output stage.

East- West pincushion correction and width adjustment are provided by a diode modulator, driven by a linear pincushion driver (Q802). U14802 IC generates the parabola used to develop the correction waveform. This allows bus control of the horizontal width and pin amplitude as well as horizontal trap correction and corner correction. In addition, a voltage developed across the high voltage return resistor (R14310) is summed at the pin driver (U14801) to compensate for the decrease in width that occurs as the high voltage increases.

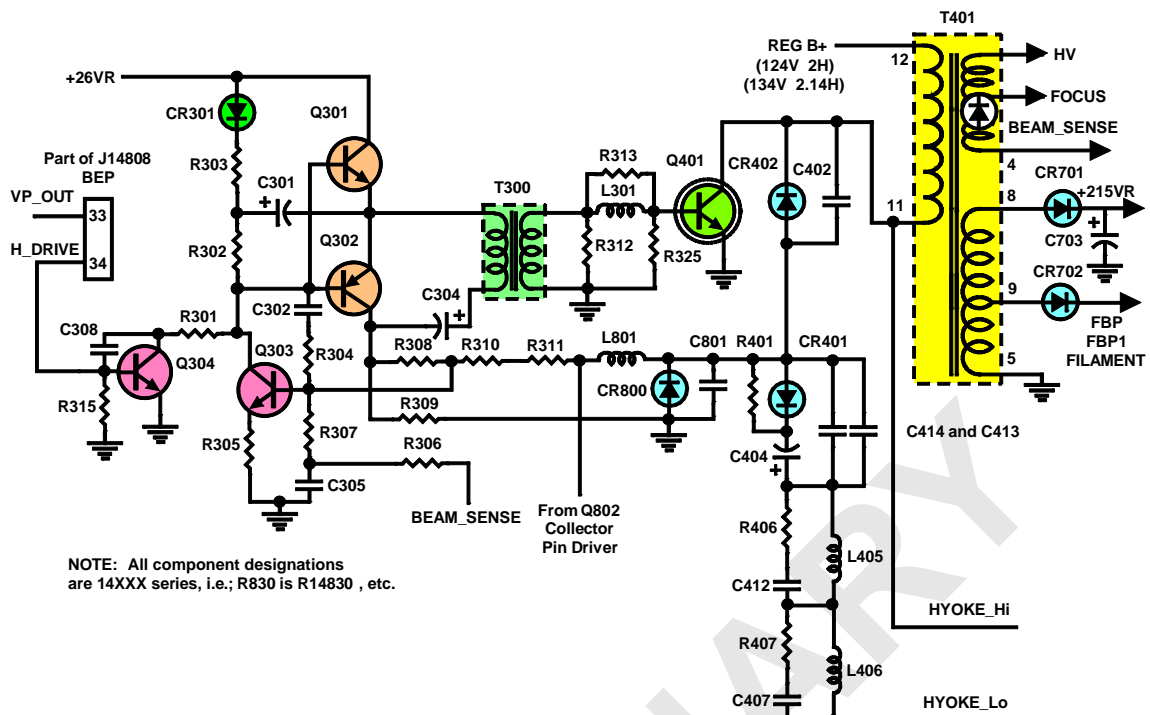
The XRP circuit in the ATC321 is similar to that of ATC311. A peak detector sets a self-biasing latch, which turns off the Main (Horizontal B+) power supply. The latch is reset by IIC communication only. The +12V detect is part of the XRP circuit called **+12V_SENSE**. A loss of the +12Vr turns on Q14701 tripping the XRP latch.

The low level vertical deflection processing is done in two parts. First the Back End Processor, that includes a sync separator and countdown circuit, provides the negative going vertical rate pulse, **VP_OUT**. This pulse is also used to synchronize the digital convergence.

Second, U14802 receives the **VP_OUT** pulse at pin 21 and develops the vertical deflection ramp at pin 6. The IC also provides a dc reference at pin 5, **VD_REF**, which tracks at twice the ramp center value. These two signals respectively become **V_RAMP** and **V_REF**, and are coupled differentially to the vertical output IC, which drives the yoke.

U14802 has an internal error amplifier with input at V_FB, pin 6 and output at V_DRIVE, pin 4, but local feedback is used to develop the reference ramp at pin 6.

Dynamic focus signals (HDF and VDF) come from U14802. Blanking signal from pin 9 of T14401 is buffered and added to the horizontal dynamic focus signal from pin 16 of U14802. The two signals are provided to the dynamic focus circuit via Q14804. Vertical dynamic focus signal comes from pin 18 of U14802.



Horizontal Out

Horizontal Out

The horizontal deflection system has two main functions in the ATC321 chassis. First, it supplies the current for the horizontal yoke. Second, it provides signals and power supplies needed for operation of the chassis and picture tube.

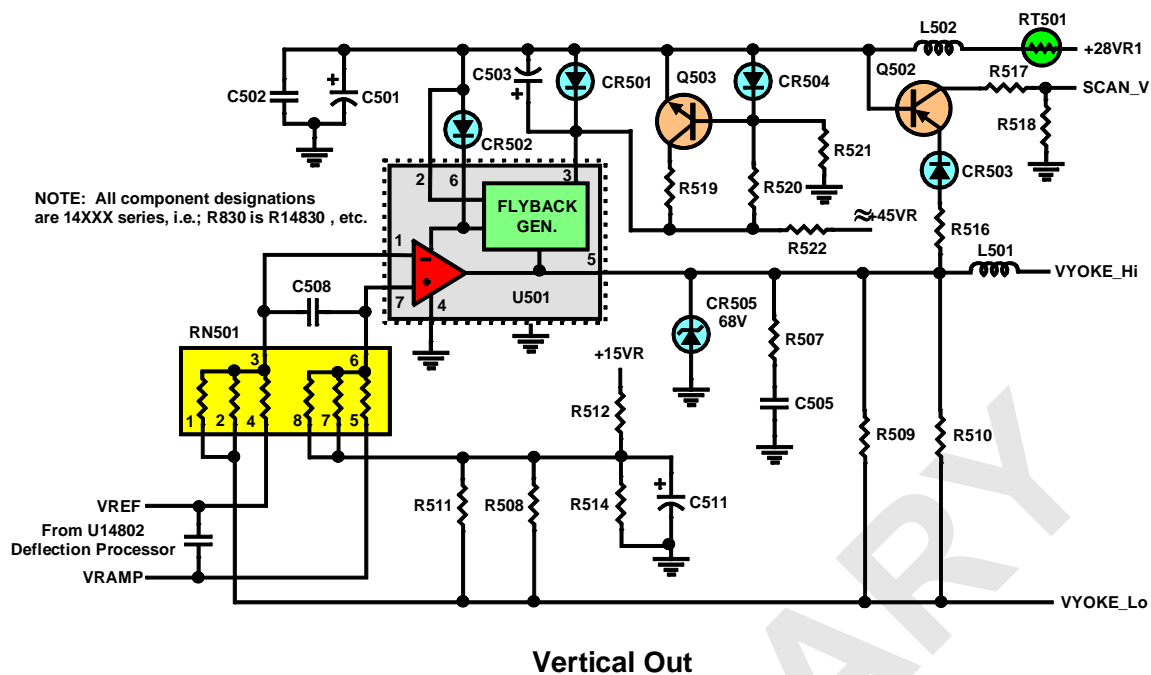
The horizontal yoke drive is provided by Q14401, CR14402, (HOT and damper diode combination), T14401 (IHVT), C14402 retrace capacitor, C14801 trace capacitor, and the horizontal yoke coils. Drive for Q14401 comes from the back end processor through J14808-34, Q14304, Q14301, and Q14302 to T14300 primary. The secondary of T14300 is inductively coupled by L14301 to Q14401-B. The frequency at which the horizontal operates is determined by the incoming signal and the BEP. The ATC311 is designed to operate at 2H and 2.14H only.

Beam sense comes from pin 4 of T14401 and is used as a control signal

for the horizontal driver and back end processor. Beam sense, at the base of Q14303, controls drive by reducing the drive signal at the collector of Q14304. As beam current increases, voltage is developed at pin 4 of T14401 and supplied to the base of Q14303. Q14303 conducts, reducing the drive signal to Q14301 and Q14302 reducing horizontal drive.

Voltages are derived from secondary windings on T14401. The video amplifier and the CRTs use these supplies. CR14701 and C14703 provide a +215V source for the CRT's and CR14702 provides the fly back pulse (FBP) for filament and timing signals. High Voltage and focus are also developed by T14401.

Pin correction signal from Q14802 is coupled to the low side of the horizontal yoke by L14801.



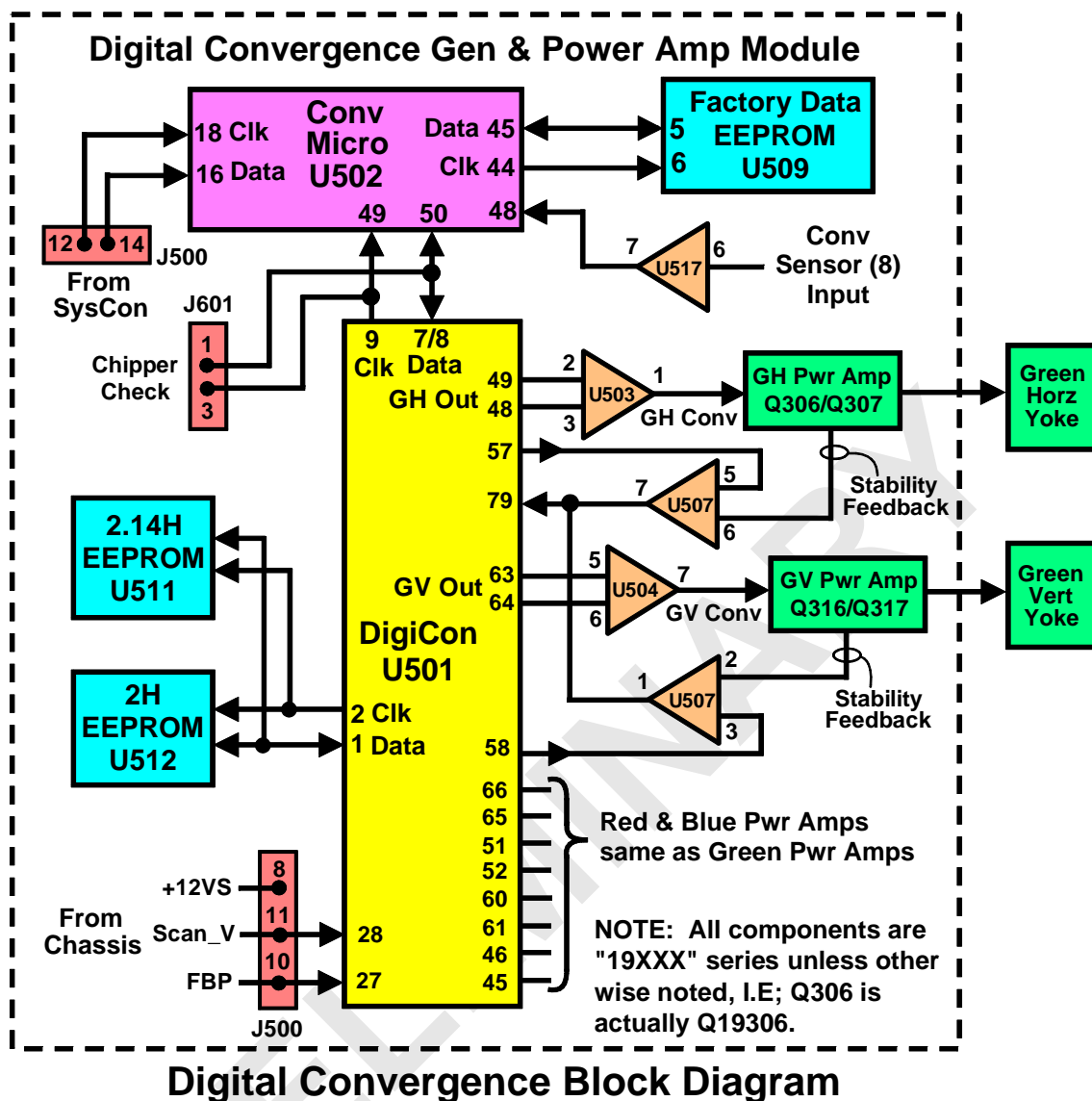
Vertical Out

The vertical output of the ATC321 is different from other vertical circuits in the past. The vertical circuit has no negative supply but uses three positive power supplies and a shunt regulator instead. The rest is similar with two signals from the deflection processor differentially coupled to U14501 via a resistor network (RN14501). These two signals are **V_RAMP** and **V_REF**. The vertical output IC (U14501) then drives the yokes. The frequency at which vertical operates is 60Hz.

Power for U14501 comes from +28Vr, +45Vr boost supply, and +15Vr half supply. The boost supply is derived from Reg B+ through dropping resistor

R1452 and shunt regulator Q14503. Shunt regulation, performed by Q14503 and the associated resistors, drops the Reg B+ voltage to +48 volts to power the output stage of U14501 during vertical retrace. The +15Vr is used as half supply with R14511 and R14508 providing current sense. C14511 provides filtering for the half supply.

A sample of the vertical output signal is used for **Scan_V**. Q14502 clamps and buffers the output signal. The signal is used for AKB and Scan Loss. If the **Scan_V** pulse is missing or distorted the video will be blanked by the Scan Loss circuit and AKB will reduce the drive. This prevents burning of the CRT's in the event vertical scan is lost.



Digital Convergence Overview

The effects of the Earth's magnetic field change with the placement of the TV and cause errors in convergence. These errors are automatically corrected using a microprocessor and data from optical sensors positioned inside around the outer edge of the screen. This process is referred to as digital convergence.

The digital convergence system generates six drive signals that correct

geometry of the image created by the three picture tubes. This is accomplished by a matrix of vertical and horizontal points that are assigned a digital value that is stored in non-volatile memory. Each of these data points can be individually changed. This stored digital information is converted into six analog signals that drive the convergence amplifiers. The amplified signals are used to drive the convergence yokes.

There are separate customer convergence adjustments along with much more detailed serviceman adjustments. The use of Chipper Check can speed up the alignment process in the event of major component failure.

There has been little change in the digital convergence when compared to the earlier projection sets with auto convergence. The ATC311 uses the same digital convergence processing and sensor arrangement as the CTC211. The ATC321 has only one scan mode, 2.14H.

The sensor position and access is the same as in the ATC311 and the process remains the same. These sensors can only be seen from the back side of the screen. A cross hatch test pattern is generated by the digital convergence micro to aid in converging the set.

Digital Convergence Generator & Power Amp Module

The ATC311 utilizes a new integrated Digital Convergence Generator & Power Amp Module for convergence correction and auto convergence. Located on the module are five EEPROMs, Convergence Micro and the Digicon IC, U501. Unlike earlier instruments, the power amplifiers are also located on the module. U502 is the convergence micro. The purpose of U502 is calculating convergence correction based on information from the optical sensors. The convergence micro controls the Digicon IC and the EEPROMs. U501 (Digicon) generates the convergence correction signals that are applied to the convergence amplifiers. U510, 511, 512, and U513 are mode EEPROMs and contain data that is used for alignment information for the different scan modes. The EEPROM U509 is the factory preset EEPROM. Two buffer ICs (U503 and 504) buffer the output from the Digicon IC to the output amplifiers. A stability feedback signal from the power amplifiers is applied to a comparator (U507) op amp along with a reference from the DigiCon IC. This is to prevent any drift of the convergence signal over a period of time due to component aging.

Horizontal and Vertical Convergence Power Amplifiers

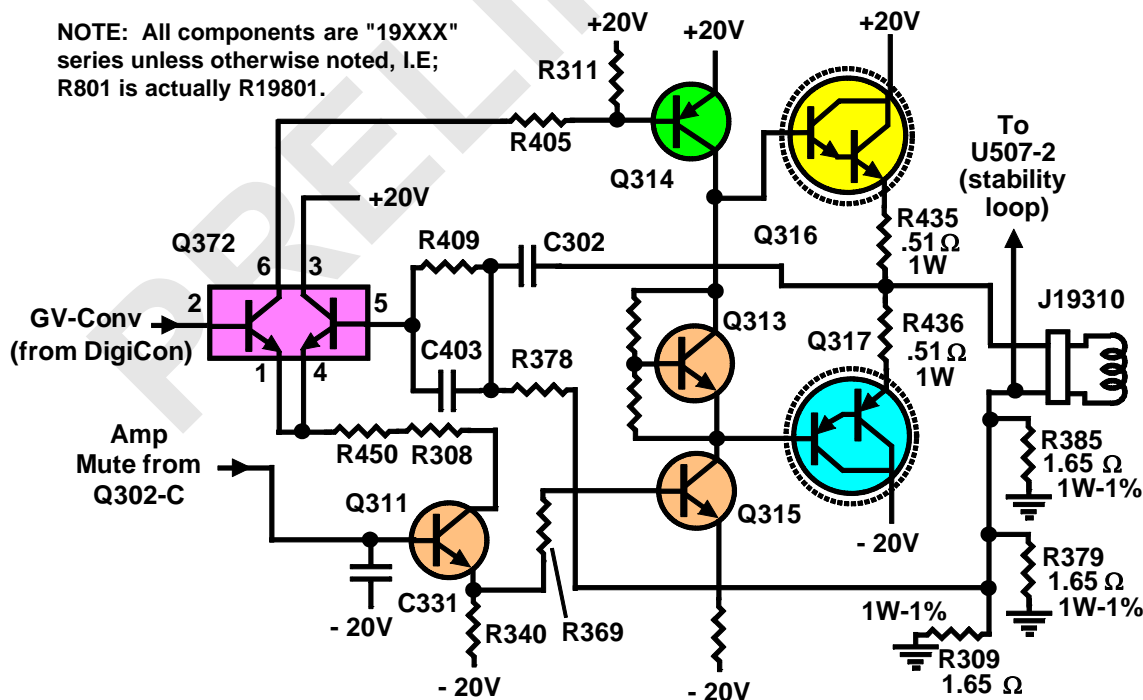
The convergence power amplifier (see Green Horz Output Amp) drives the convergence yokes via the drive waveform (GH-Conv) at pin 2 of Q370 from the DigiCon IC. The power amplifier operates between +/-20V supplies. The voltage across the yoke current sense resistors consisting of three 1.65 ohm resistors (R442, 441 & 301) is applied to the stability loop circuit of U507-6. This voltage also serves as a feedback voltage to pin 5 of Q370. Q370 is provided a fixed current (at pins 1 & 4) by a current source (Q301) that is biased on or off by a mute switching voltage (1.8V-On or 0-Off) that is output from the DigiCon IC U501, pin 77.

All the convergence power amplifiers are turned off during power up and convergence data loading from the EEPROM. The transistor Q301, a current source transistor is also an emitter follower that drives the negative pre-driver transistor (Q305). The positive rail pre-driver (Q304) is driven by the left side transistor (pins 1, 6) of

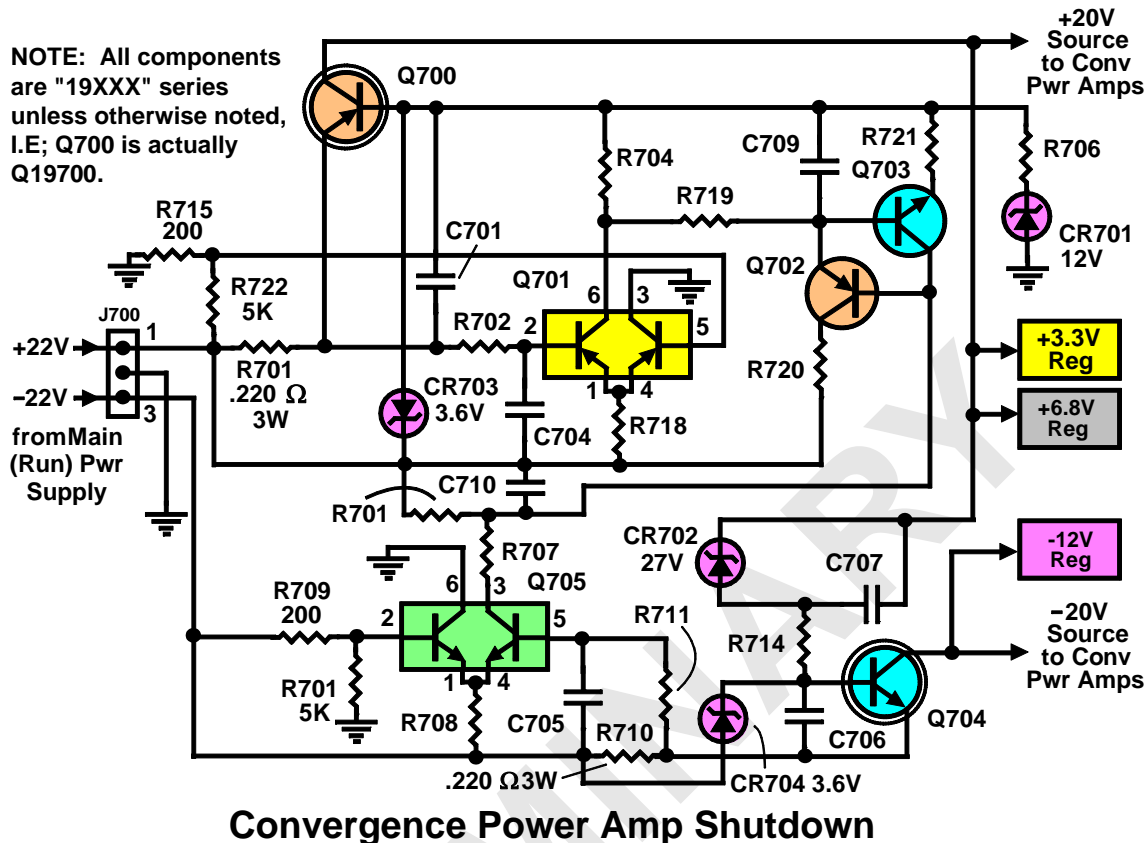
Q370. The pre-driver transistors Q304 and Q305 provides the drive for the NPN and PNP power Darlington transistors (Q306 & Q307). These power transistors operate in class B mode and drive the high side of the convergence yoke. Feedback from the high side of the yoke is coupled to pin 5 of Q370 and sets phase margin and damping. A sample of the voltage across the sense resistors is also sent to comparator (U507-6). These levels are compared with standardized outputs from the DigiCon IC U501. The DC balance and AC gain of each of the 6 channels is digitally adjusted to correct for any drift. The vertical amplifiers (see Green Vert Output Amp) are almost identical but have a transistor (Q313) connected as a base to emitter voltage multiplier located between the bases of the power Darlington. Also, feedback resistors R434 and R435 are included in series with the Darlington emitters. These two changes reduce the class B crossover transients and eliminates a horizontal streak from the raster.

NOTE: All components are "19XXX" series unless otherwise noted, I.E; R801 is actually R19801.

Green Horizontal Convergence Output Amp



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Convergence Power Amplifier Shutdown

The convergence power amplifier shutdown circuit is designed to prevent further damage to the power amplifiers by removing the $\pm 20\text{V}$ supplies in the event of a failure. Q700 and Q704 act as disconnect switches while Q702 and Q703 serve as a latch. The latch resets when the set is cycled off and back on. Q700 and Q704 disconnects the power supplies to the convergence amplifiers and latch them off via Q702 & Q703 if either supply delivers greater than 3A for more than 10 to 15mS. The delay is needed because of startup current spikes. It's important to realize that all the bias voltages in the circuit are provided by the $\pm 22\text{V}$ supply from the

main (run) power supply. Transistors Q700 and Q704 actually provide the $\pm 20\text{V}$ source supply to the convergence power amplifiers.

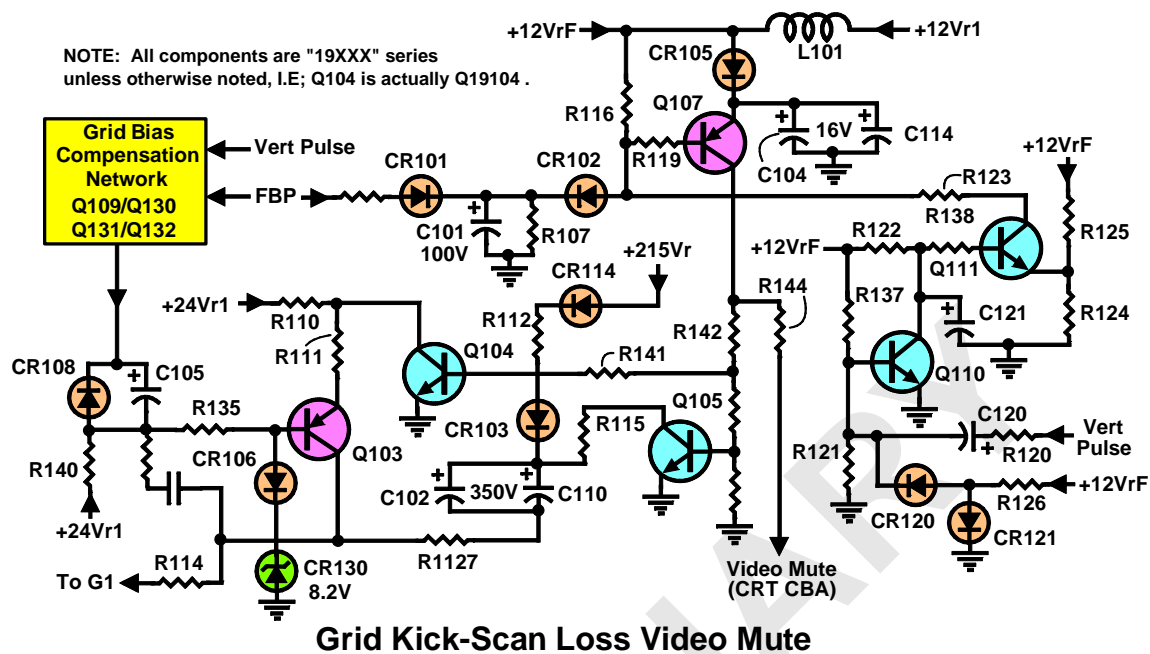
During normal operation Q700 is biased On by CR703, R706 and CR701. Also, during normal operation transistor Q701 pins 1-2-6 is biased Off. R701 serves as the current sense resistor. As current increases through R701 the voltage at pin 2 of Q701 begins to fall. The voltage at pin 5 of Q701 is a reference voltage provided by R715 and R722 and determines the voltage at which the transistor Q701 (pins 1, 2 & 6) turns on.

It's important to note that the R/C time constant of R702 and C704 provides the 10 to 15mS delay. C704 holds pin 2 of Q701 Hi for 15mS before letting the transistor turn on. When the voltage falls to .7V below the emitter (pin 1), the transistor turns on applying a Hi to the base of Q703 turning it on. When Q703 turns on Q702 turns on and they latch. With Q703 on, a Hi is placed on the base of Q700 by the emitter voltage of Q703 turning Q700 off and removing the +20V source from the power amplifiers. With the +20V source gone, the base of Q704 is allowed to go more negative than the emitter thus turning it off. With Q704 off, the -20V source is removed from the convergence power amplifiers.

The negative side of the circuit (Q704 and Q705) operates in the same manner as the positive side except that the voltages are below ground potential. When excess current is drawn from the

-22V supply through R710, the base voltage at pin 5 of Q705 goes Hi enough for the transistor to turn on. With Q705 on, the base of Q702 (latch circuit) is pulled Lo enough for it to turn on. With Q702 on, Q703 turns on and again places a Hi on the base of Q700 removing the positive source voltage. With the +20V at the cathode of CR702 missing, Q704 is biased off removing the -20V source. C705 and R711 provides the 10 to 15mS delay in the negative circuit.

The +20V source is also applied to a +3.3V regulator located on the convergence circuit board. This +3.3V supply is for the DigiCon IC and the convergence microcomputer. If the +20V source is lost, the +3.3V is also lost and the convergence microcomputer goes down. When the system control micro tries to communicate with the convergence micro it does not get a reply and system control micro shuts the instrument down.



Grid Kick/Scan Loss Video Mute

The grid kick/scan loss video mute circuit has three (3) primary functions. One is to provide bias for the G1 grid of the picture tubes. Two, adjust grid bias from +10VDC to approx. +24VDC during horizontal and vertical blanking (retrace). This is done to compensate for any breathing (fluctuation) of the 'unregulated' high voltage power supply. Third, horizontal and vertical are monitored for scan loss. If horizontal or vertical are lost, the G1 grid is reverse biased at approximately -180VDC to prevent burning the tubes and video is muted.

During normal operation (horizontal and vertical scan) transistor Q103, diode CR106 and zener CR130 provide bias of approximately +10VDC to grid G1. During horizontal and vertical blanking

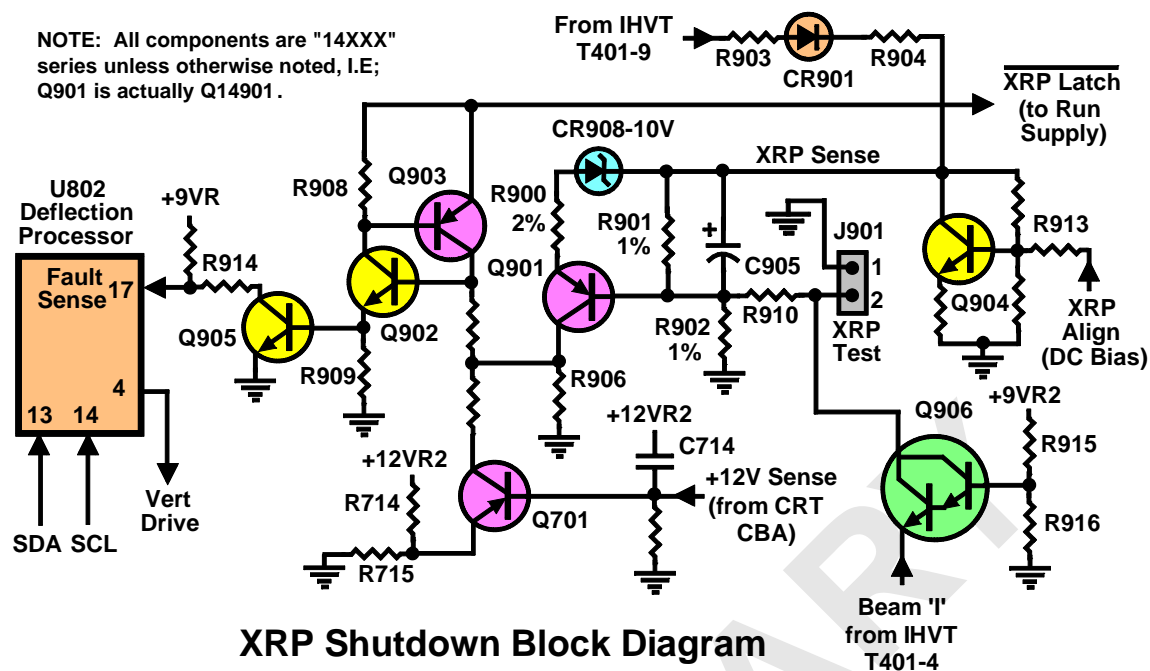
(retrace) the grid bias compensation circuit (Q109/130/131/132) drives the base of Q103 turning it on harder. This drives Q103 collector (G1 bias) to approximately +24VDC. In this way the grid to cathode bias remains proportional during any high voltage fluctuations.

Horizontal scan loss detection is performed by rectifier diode CR101 and filter capacitor C101. Whenever the flyback pulse (FBP) is present diode CR101 and capacitor C101 act as a rectifier and generate a positive DC voltage that is applied to the cathode of CR102 reverse biasing it. With CR102 reverse biased, transistor Q107 is held off allowing normal scan. If horizontal scan is lost, C101 is discharged through R107. CR102 is forward biased via

R107 and R116 placing a low on the base of Q107 turning it on. With the loss of horizontal, the run supply is lost and the voltage stored in capacitors C104 and C114 provides the B+ for Q107. With Q107 turned on Q104 and Q105 are turned on. The grid kick voltage (approx. -180VDC) is generated by capacitors C102 and C110 charging through diode CR103 and CR114 to the +215V supply. When Q105 turns on, the positive side of the grid kick capacitors are grounded applying a negative 180VDC directly to the G1 grid. Reverse biasing the G1 grid with -180VDC ensures that the cathode current is zero. At the same time Q104 is turned on grounding the junction of R110 and R111 and turning off the +10V grid bias by removing B+ from the emitter of Q103. A high (video mute) is

also coupled to each CRT circuit board via R144.

Vertical is monitored for scan loss by Q110 and Q111. A vertical pulse is capacitively (C120) coupled to the base of Q110. CR120, CR121 and the +12Vr provides bias to the base of Q110 causing it to act as a vertical rate oscillator. With Q110 oscillating, the base voltage of Q111 is kept low enough to keep it off. When vertical is lost, capacitor C121 charges through R122 and turns on Q111. When Q111 turns on, the base of Q107 is pulled low turning it on. This applies a high to Q104, Q105 and also to the CRT CBA's (video mute). As with horizontal loss, Q105 applies the grid kick voltage (-180VDC) to grid G1 and Q104 shuts off the grid bias transistor Q103.



XRP Shutdown Overview

The primary function of the XRP circuit is to turn off the run power supply and shutdown the deflection processor IC, U802. The XRP shutdown circuit has three (3) inputs. These are the Over-Voltage, +12V Sense (CRT CBA) and the excessive beam current. Detecting over-voltage is performed by CR901 and CR908. A horizontal pulse from the IHVT T401 pin 9 is rectified by CR901. A precision reference voltage is generated by Q904 and the XRP Align bias voltage. This XRP Align voltage is stored digitally in the EEPROM and is converted (by a DAC) to an analog

voltage. When the voltage on the cathode of CR908 (Q904-C) rises above 10V, zener CR908 breaks over and transistor Q901 turns on. With Q901 turned on, the latch (Q902 & Q903) turns on and outputs a low (XRP Latch) that turns off the run power supply (see run power supply). When Q902 turns on, the base of Q905 is pulled high enough to turn it on. With Q905 on, a low is applied to pin 17 of U802, instructing it to turn off vertical and send a message to the system control (SDA) to shutdown the instrument.

The +12V Sense monitors for problems in the video drive circuit on the CRT CBA's to prevent damage to the CRT's. In the event the video drive IC shorts or the 215V cathode voltage is lost the XRP circuit is activated, shutting down the instrument. The CRT CBA +12V Sense is applied to the base of Q701. Q701 is held off as long as the +12V is present. If the +12V is lost on the CRT circuit board, the base of Q701 goes low enough to turn on Q701. When Q701 is on, the latch circuit (Q902/903) turns on again and applies the XRP

Latch signal to the run supply. Also, Q905 turns on shutting down U802.

Beam current is monitored by Q906. The emitter of Q906 is connected to pin 4 of the IHVT, T401. When excessive beam current occurs the emitter voltage of Q906 is pulled below its base voltage which turns it on. With Q906 on, a low is applied to the base of Q901 turning it on. With Q901 turned on the latch Q902/903 turns on generating the XRP Latch. Q905 also turns on shutting off IC U802.

PRELIMINARY

Appendix A

Troubleshooting Section

Dead Set Troubleshooting

NOTE: If power LED comes on when power button is pressed and then the set powers down (LED off) go to step 6.

1. Use BP204-1 as the hot ground reference. Check Raw B+ at connector BP204-2 (AC IN CBA). If Raw B+ is OK, go to step 4. If not OK go to step 2.
2. Check AC fuse, FP201. If fuse is OK, suspect AC IN CBA. If fuse is open, unplug horizontal yoke plug J14401 (Deflection CBA) and check for short between pins 1 and 2 on the deflection circuit board. If shorted suspect Deflection CBA. If not shorted go to next step.
3. Use the interconnect diagram as a reference and BP603-10 as the cold ground reference. Check all standby voltages at connectors BP603, BP602, (AC IN CBA). If any standby voltages missing, suspect AC IN CBA. If standby voltages are OK go to next step.
4. Apply AC power and press power button.
5. If LED turns on and then off, disconnect J11501 (Audio CBA) and press power button again. If power LED comes on and stays on suspect Audio CBA. If LED still flashes or does not light go to step 7.
6. Disconnect BP602 (AV IN CBA) and press power button again. If power LED comes on and stays on suspect AV IN CBA. If LED still flashes or does not light go to next step.
7. Disconnect J19500 (Convergence CBA) and press power button again. If power LED comes on and stays on troubleshoot the Convergence CBA. If LED still flashes or does not light go to next step.
8. Disconnect J14801 (Deflection CBA) and press power button again. If power LED comes on and stays on suspect Deflection CBA. If LED still flashes or does not light suspect DM3 module.

Standby Power Supply Troubleshooting

1. With AC power supplied, check for raw B+ at connector BP204-2. If raw B+ is ok, go to step 4. If not ok, check FP201, DP201, CP208 and 209.
2. If fuse FP201 is open, remove AC power, unplug J14401 and check for short between pins 1 and 2 on the deflection CBA side. If shorted troubleshoot the run supply and deflection circuits. If not shorted, go to step 3.
3. Remove AC power and check TP601 for gate to drain short and drain to source short. If shorted replace all active components on the primary side of LP601 and RP601. If not shorted, go to step 4.
4. Unsolder drain of TP601, if fuse was open replace AC fuse and apply AC power.
5. Check for +12Vdc on the gate of TP601. If missing, suspect RP604, 605, 602, DP601, 602, TP602, and 601. If +12Vdc present, go to step 6.
6. Remove AC power and check for proper resistance (see table on pg. 30) on each output diode DP620, 623, 626, 630, 637, and 638. If not correct check associated circuit with each incorrect resistance. If resistances are ok, go to step 7.
7. Solder drain of TP601 back in, short pins 3 and 4 of IP601, and apply AC power. If supply starts to oscillate, check IP601, 602, and precision resistor network in feed back circuit. If not check components in the source circuit of TP601.

Standby Power Supply Resistance Table

DP610	Infinity
DP613	5K
DP612	85 ohms
DP614	115 ohms
DP615	2K
DP616	2K

Run Power Supply Troubleshooting

No Start, Relay clicks, and Power LED is on

NOTE: If relay clicks and power LED comes on then the standby power supply and system control are functioning.

1. Apply AC power and check Q14101-D for raw B+ (approx.150Vdc). If missing, check J14101 from the standby supply and T14101 for an open circuit. If raw B+ is correct go to step 2.
2. Remove AC power, unsolder the drain of Q14101 and short collector to emitter of on/off transistor Q14150. This will turn on bias to the oscillator circuit and gate of Q14101. Check for +24V on the Q14101-G. If missing check Q14102, 103, 151, R14103, 104, 105, 106, 107, CR14113, and CR14114. If +24V present, go to step 3.
3. Using the resistance table, check each output diode. If resistances are correct go to step 4. If not correct check associated circuit of improper resistance reading.
4. With Q14150 still shorted (C-E), solder the drain of Q14101 back in and short pins 3 and 4 of U14101 to bypass regulation control. This makes the supply operate at reduced voltage. Apply AC power, if supply starts to oscillate, check feedback circuit Q14104, U14103, U14101, and precision resistors. If no oscillation, go to step 5.

5. Remove AC power and check components off of pin 11 of T14101 and off of pins 3 and 4 of U14101. Check components in the source circuit of Q14101.

Resistance Table

CR14109	55K
CR14108	9K
CR14107	28K
CR14106	Infinity
CR14140	5K
CR14142	5K

System Control Troubleshooting

Dead set, isolate down to chassis or DM3 module. Power LED blinks.

1. Apply AC power and check J13604 and J13605 for proper voltages all pins. Voltages not correct troubleshoot AC in CBA. Voltages correct go to step 2.
 2. Check J13604-1 for 5Vdc. If missing or low power supply is indicating power failure. Troubleshoot AC in CBA. If 5Vdc ok, go to step 3.
 3. Remove AC power and disconnect J14801 on the deflection CBA. Apply AC power and turn on set. If power led turns on, troubleshoot deflection CBA. If power LED still wont stay on suspect DM2 module.
-

Horizontal Out Troubleshooting

Setup:

- Unsolder Q14401-C
- Disconnect all three CRT sockets
- Force on Run supply by shorting C-E on Q14150
- Force on 9Vr for BEP by shorting C-E on Q14111 and apply AC power.

Horizontal Drive should be present at pin 34 of J14808 if not troubleshoot BEP.

1. Check for drive signal at Q14304-C. If missing check +26Vr, Q14304, and Q14303. If ok go to step 2.
2. Check for horizontal drive at Q301-E. If missing check base circuit of Q14302 and Q14301, 14302, and C14304. If ok go to step 3.
3. Check for signal at the base of Q14401. If missing suspect Q14401, T14300, and L14301. If present, remove AC power and reconnect Q14401-C.
4. Unplug J14401, horizontal yoke.
5. Apply AC power and check for signal (490V P-P) at the collector of Q14401. If incorrect, suspect T14401 or it's secondary circuits. If correct suspect yokes or yoke return circuit.

Vertical Out Troubleshooting

Troubleshooting Tips

- If there is no vertical pulse from U12901-27, confirm fly-back pulse is present at U12901-24. It must be present for the vertical countdown to function.
- If the vertical power stage U14501 has failed, CR14501 has likely failed also, and should be replaced. Failure to replace it will result in the boost voltage being equal to the 28VR1 supply voltage. The retrace will be too slow, and SCAN_V will not be proper. AKB blanks the picture if this pulse is not proper.

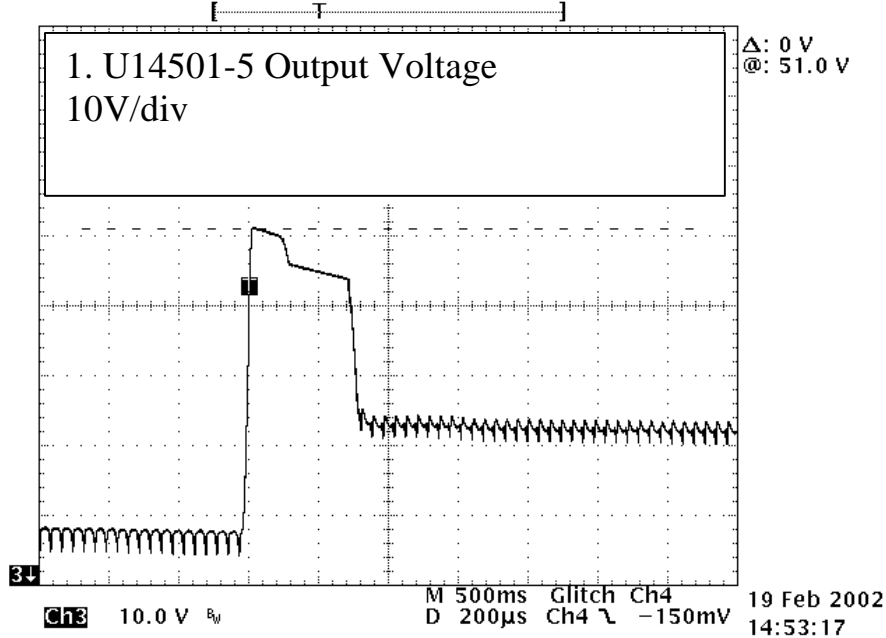
1. Disconnect CRT sockets from all three CRT's.
2. Disconnect vertical yoke plug J14501.

3. Apply AC power and turn on set.
4. Check Source voltages +28Vr, +15Vr, and +45Vr. If sources are missing troubleshoot source supplies. If ok, go to step 5
5. Check U14501 for proper voltages at pins 1, 2, 3, 5, 6, and 7. See chart below. If incorrect, suspect U14501, CR14501, RN14501, and C14503. If correct, go to step 6.
6. Check for waveform at pin 5 of U14501. If correct suspect open yoke. If not correct suspect R14509, 14510, and feed back components to RN14501.

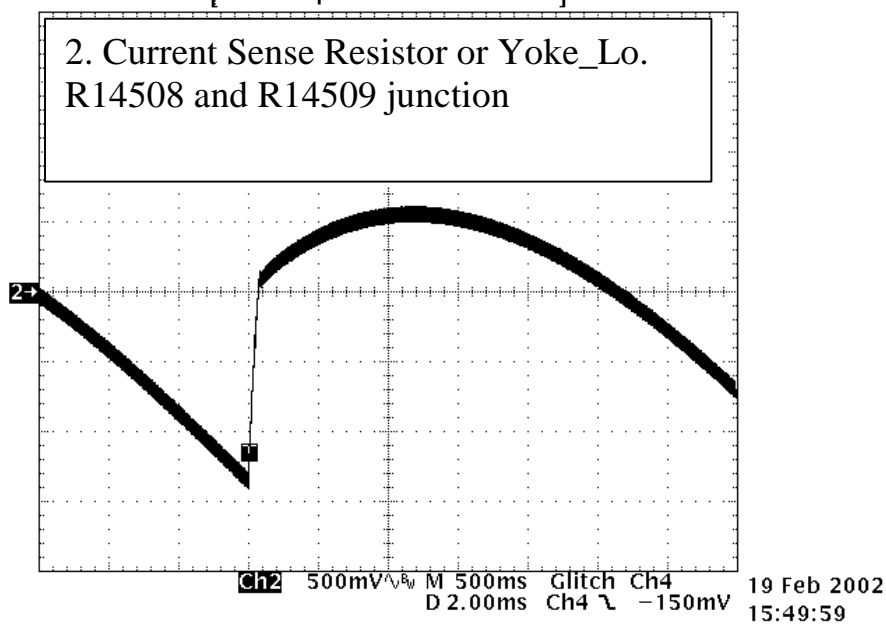
U14501 Pin #	Voltage With Yokes	Voltage W/O Yokes
1	7.9Vdc	7.9Vdc
2	31.5Vdc	31.5Vdc
3	46.8Vdc	47.3Vdc
5	15.1Vdc	15.8Vdc
6	30.9Vdc	31.0Vdc
7	7.8Vdc	7.8Vdc

Vertical Key Waveforms

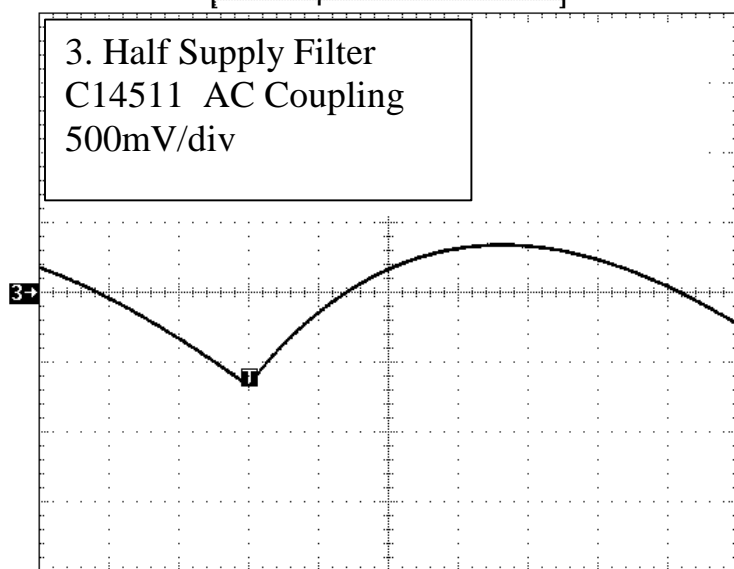
Tek Run: 25.0MS/s Hi Res



Tek Run: 2.50MS/s Hi Res



Tek Run: 2.50MS/s Hi Res

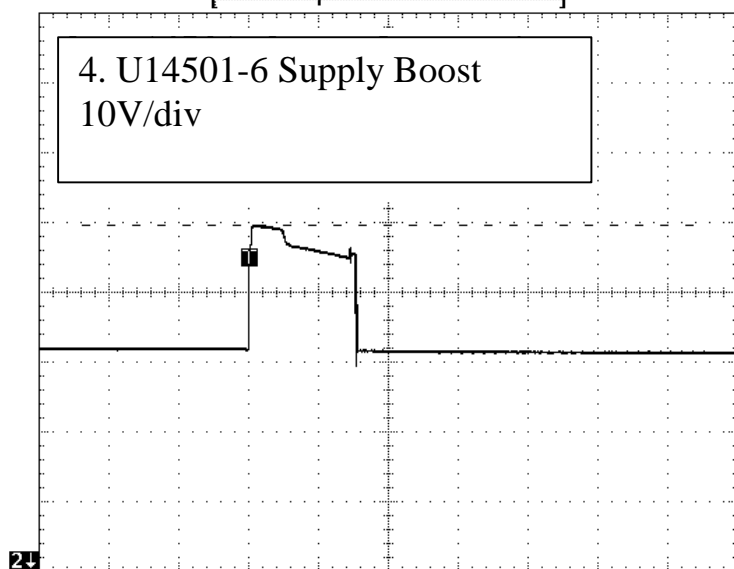


Ch3 500mV/V_B

M 500ms Glitch Ch4
D 2.00ms Ch4 -150mV

19 Feb 2002
15:50:42

Tek Run: 25.0MS/s Hi Res



2↓

Ch2

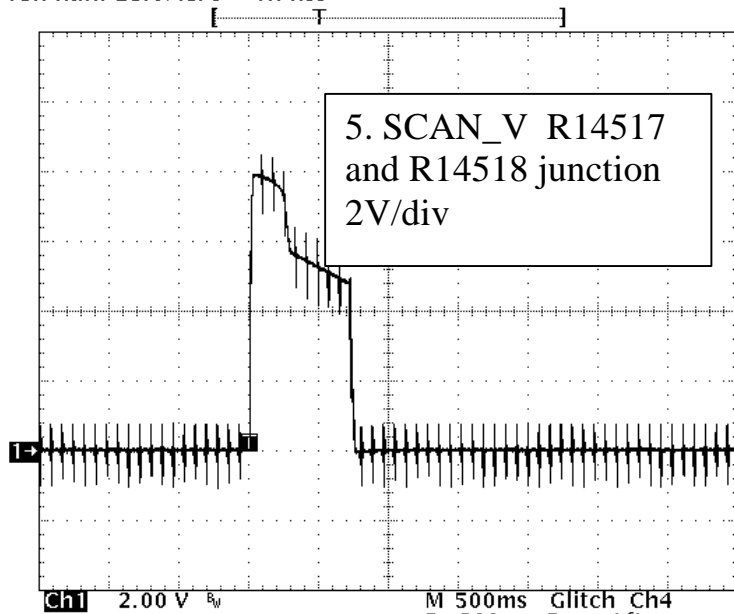
10.0 V

M 500ms Glitch Ch4
D 200μs Ch4 -150mV

Δ: 0 V
@: 49.6 V

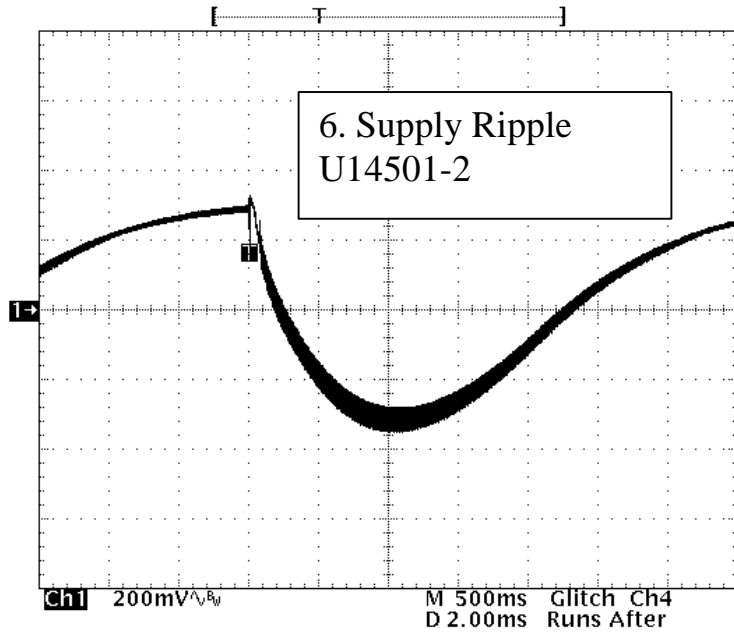
19 Feb 2002
14:51:59

Tek Run: 25.0MS/s Hi Res



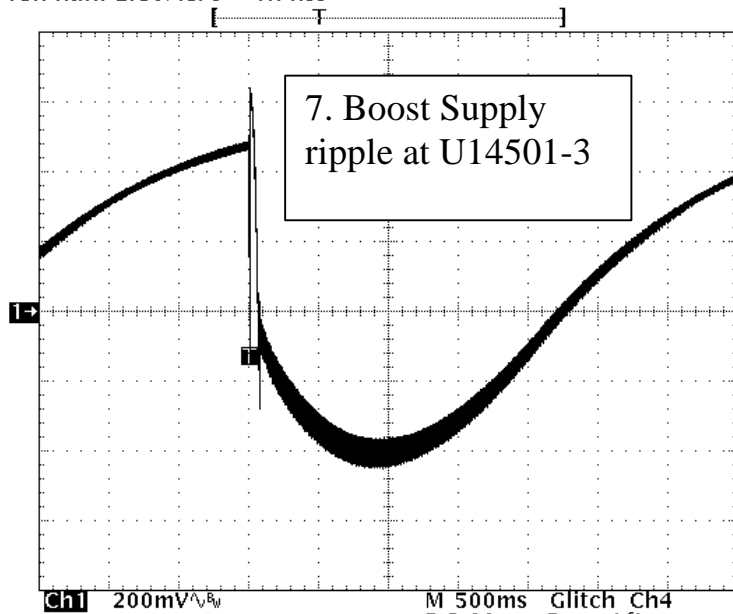
21 Feb 2002
16:00:07

Tek Run: 2.50MS/s Hi Res



22 Feb 2002
07:55:14

Tek Run: 2.50MS/s Hi Res



21 Feb 2002
15:56:22

XRP Shutdown Troubleshooting

1. Remove CRT CBA's. Apply AC power and turn set on. If set starts suspect +12V Sense and/or excessive beam current shutdown.
 2. If set doesn't start with CRT sockets unplugged, remove R14914 (XRP bypass). Monitor high voltage and turn set on.
 3. If high voltage is excessive, troubleshoot horizontal and Reg B+ circuits.
 4. If high voltage is OK, suspect component failure in XRP circuit.
-

Back End Processor Troubleshooting Tips

If there is video at the input, but no RGB output, check that the FSW0 line, pin 20 of J12901 connector, FSW0 is low. If it is high, the video will be blanked.

If there is video at the input, but no RGB output, check that the BLK_OUT line, pin 25 of the J12901 connector is low. If it is high, video will be blanked.

Troubleshooting No Video any mode

1. Check for clock and data at J12901-1 and 2. If missing troubleshoot deflection CBA and DM2 clock and data lines. If ok, go to next step.
 2. Select a known good channel and check for proper signals on J12901-5, 6, 7, 8, and 9. If missing, troubleshoot DM2 and A/V switching CBA. If correct, go to next step.
 3. Check for proper signals at J12901-28, 29, and 30. If correct, troubleshoot deflection CBA, CRT CBA for loss of signal flow. If missing, see troubleshooting tips above and suspect BEP.
-

Convergence Generator Troubleshooting

1. Check the operation of the Convergence Power Amps and the Convergence Power Amp Shutdown circuits using the appropriate troubleshooting procedure. If the circuits check OK go to next step.
 2. Check clock and data at J19500 pins 12 & 14. If OK go to next step. If not OK suspect loss of clock and data between system control and convergence CBA.
 3. Check for +12VS at J19500-8. If OK go to next step. If not OK, troubleshoot +12VS standby supply.
 4. Check J19500-10 & 11 for horizontal and vertical sync. If OK suspect convergence CBA. If not OK, troubleshoot horizontal and vertical sync circuits.
-

Convergence Power Amplifier Troubleshooting

1. Remove AC power and unplug convergence yokes. Apply AC power and turn instrument on. Check for the +/-20VDC supplies at collectors of output transistors, IE; Q19306 and Q19307.
2. Check emitter junction of power output devices for 0VDC. If other than 0VDC, suspect power amplifier circuit.

NOTE: Pre-drivers and output devices may be swapped with like components of other power amp circuits to verify defective devices.

Convergence Power Amplifier Shutdown Troubleshooting

1. Remove AC power and disconnect J19500. Apply AC power and start instrument. If chassis starts go to next step. If chassis doesn't start go to Dead Set Troubleshooting.
 2. Remove AC power and disconnect J19310 and J19311 (convergence yokes). Apply AC and turn instrument on.
 3. Check Q19704-C. If +20VDC present, check Q19704-C for -20VDC. If OK, troubleshoot convergence power amplifiers. If not OK, go to next step.
 4. Check for +/-22VDC at J19700-1/3. If missing troubleshoot the main (run) power supply. If OK, suspect a problem in the amplifier shutdown circuit (static check all components).
-

No Video Troubleshooting

1. Apply AC power and turn on unit.
2. Press menu, if OSD is present go to step 6.
3. No OSD / video, connect 2H or 2.14H Y Pr Pb signal to Aux. 4 input and using the remote slowly cycle through all inputs. This requires pressing the input button on the remote seven (7) times to cycle through all inputs.
4. Video present and no OSD go to step 8. No video present, go to next step.
5. Using scope check for signals on J14802-1, 2, 4, 6, and 8. Signals present, suspect deflection / back end processor. Signals not present suspect AV In CBA.
6. Using a known good NTSC RF source and splitter, connect source to both antenna inputs. Check for video on antenna A and B, if no video on both or

just one antenna input suspect DM3. If video is present with both antenna A and B go to next step.

7. Connect a NTSC 1H video signal to aux inputs. Cycle through each of the inputs. No video or video on some inputs, suspect AV In CBA.
 8. Using a video monitor connected to the video output, tune to an active station. Video displayed on monitor suspect A/V In CBA. No video displayed suspect DM3 module.
-

PRELIMINARY

TTE

RCA SCENIUM